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(54) APPARATUS FOR DISPLAYING A COMPUTING FUNCTION

(71) We, MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD., a corporation organized under the laws of Japan of 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to apparatus which can display in a plurality of rows on the picture tube of a television receiver the results of a computing process that is carried out in a computing section, i.e. electronic table calculator (hereinafter referred to as ETC for brevity) associated with the television receiver.

The kind of electronic table calculator or ETC now on the market can display the computed result only in a single row by utilizing fluorescent display tubes, Light Emitting Diodes or liquid crystal cells. In such an ETC, therefore, it is difficult to display the computing process.

According to the present invention there is provided an apparatus for displaying a computing process comprising a computing means for performing a computing operation on input data, a memory means for storing the input data and result of the computing process performed by said computing means, a means for reading the contents of said memory means and converting said contents into character, representative video signals, a means for receiving a television signal and demodulating the video signal in the received television signal, a picture tube operated to display thereon images by receiving said character representative video signals and the signal from said receiving and demodulating means, wherein the images representing the charcater representative video signals and the demodulated video are displayed in superimposition on the picture tube, a driving means which receives a first synchronizing signal obtained from said computing means and a second synchronizing sigal separated from said television signal and which applies to the memory means driving pulses timed in relation to the timing either of said first synchronizing signal in the case of writing into said memory means or of said second synchronizing signal in the case of reading of the contents of said memory means.

For better understanding the present invention reference may be had to the accompanying drawings, in which:—

Fig. 1 is a block diagram of apparatus according to the present invention;

Fig. 2 is a block diagram of a data converting circuit;

Fig. 3 comparatively shows the content of an operational register and that displayed on the picture tube;

Fig. 4 is a block diagram of a display control circuit;

Fig. 5 is a timing chart of a line display circuit;

Fig. 6 is a block diagram of a spacing circuit;

Fig. 7 is a timing chart for the spacing circuit shown in Fig. 6;

Fig. 8 shows timing charts of a character generating circuit and a parallel-series register and the pattern of a numeral;

[Price 33p]

Fig. 9 is a block diagram of a color control circuit;

Fig. 10 shows how numerals necessary for one computation are displayed on the picture tube; and

Fig. 11 shows step by step the variations of display according to the progress of the computation.

In Fig. 1, constituents enclosed by the dashed lines 78 constitute an electronic table calculator ETC, which comprises an input unit or key board 1, an input control circuit 2, a computation control circuit 3, and an operational register 4. A data converting circuit 5 which writes thereinto the content of the operational register 4 in timing with the ETC and reads out data onto a picture tube 18 in response to a synchronizing signal separated from a received television signal by a television receiver 79. A character generating circuit 6 converts the outputs 36, 37, 38 and 39 of the data converting circuit 5 into address signals, signals 31, 32 and 33 (from a display circuit 8) into a signal for selecting a row where a certain character is to be displayed, and the signals 34 and 35 from the input unit 1 of the ETC 78 into address signals for operators. A parallel-series register 7 receives the parallel data 51, 52, 53, 54 and 55 from the character generating circuit 6, and decimal point data 41, a clock signal 30 and a load signal 40 from the display circuit 8, and delivers an output signal 43. The display control circuit 8 supplies positioning signals 26, 27, 28 and 29 to the data converting circuit 5 and a color control circuit 9, for properly positioning the data on the picture tube in response to horizontal and vertical synchronizing signals 46 and 47. Signals 31, 32 and 33 for selecting a row in which each character or numeral is displayed are fed to the character generating circuit 6 and a line signal 42 is applied to the color control circuit 9. A dash line enclosure 79 indicates a part of an ordinary television receiver, which comprises an antenna 56, a tuner 10, a video IF amplifier 11, a video detector 12, a first video amplifier 13, a synchronizing circuit 14 for supplying the horizontal and vertical synchronizing signals 46 and 47 for the display control circuit 8, a color synchronizing circuit 15, a demodulator 16, a matrix circuit 17, and a picture tube 18 to which red, green and blue chrominance signals 48, 49 and 50 are fed from the matrix circuit 17. These chrominance signals together with the outputs 44 and 45 of the color control circuit 9 can produce a color display on the picture tube 18.

The operation of the circuit shown in Fig. 1 will next be described. A numeral signal from the input unit 1 of the ETC 78 is processed by the input control circuit 2 and the computation control circuit 3, stored in the operational register 4, fed as a signal 19 to the data converting circuit 5, sequentially memorized in the register included in the circuit 5 such that it will be read out from the most significant digit down (described later in detail) read out from the register upon the completion of the memorization in response to the clock signal 30, further fed through the character generating circuit 6, the parallel-series register 7, the color control circuit 9 and the matrix circuit 17, and finally displayed on the picture tube 18. On the other hand, the operator is displayed by directly applying the signals 34 and 35 from the input unit 1 to the character generating circuit 6. Another numeral positioning signal written in the register 7 is also displayed on the picture tube 18 in the same manner as described above, all the process of computations so far displayed with the first operand, and the operator and second operand appearing respectively in the second and third rows. Then, if the equality button of the input unit 1 depressed, the computed result is written in the register 7 and at the same time the line signal 25 is supplied for the display control circuit 8 so that the signal 42 is applied to the color control circuit 9. Therefore, the first operand, operator and second operand, a horizontal line, and the computed result are displayed on the picture tube 18. When a series of computations are continuously performed, this process of display will be repeated.

Fig. 2 shows in detail the constitution of the data converting circuit 5. This data converting circuit 5 receives the information from the ETC 78 which is derived serially from the least significant digit upwards, and writes the information into the memory circuit in such positions that it may be read out from the most significant digit down, so that the desired information is properly displayed on the picture tube 18. In Fig. 2, there are shown a register selecting circuit 57, a memory circuit 58 consisting of registers SR1, SR2, SR3, and SR4 each adapted to store $4 \times n$ bits (where every row consists of n-digits and each digit is represented by bits), a register 59 for series-parallel converting a part of the data corresponding to one digit (4 bits), a scale-of-n counter 63, a change-over control circuit 64 for switching over the writing and reading of the memory circuit 58, a clock drive circuit 60, NAND circuits NA1 . . . NA9, a scale-of-four counter 61, and a scale-of-(n—1) counter 62. The information 19 from the ETC 78 is controlled by control signals 20 and 21 and a busy signal 22, and written selectively into respective registers of the memory circuit 58 in the computing order. The clock signal to the memory circuit 58 is the NAND taken at the circuit NA1 of the output of the change-over control circuit 64 and the clock pulse

signal 23 from the ETC 78, and the clock signal 23 is also applied to the scale-of-four counter 61 connected with the scale-of-(n−1) counter 62. Therefore, the gate of the NAND circuit NA2 is opened every time 4(n−1) clock pulses of the signal 23 have been counted, so that four clock pulses are applied to the clock drive circuit 60. Accordingly, clock signals ϕ_1 and ϕ_2 are produced and a piece of information corresponding to a single digit in the operational register 4 of the ETC 78 is serially written in one of the registers SR1 to SR4 of the memory circuit 58. Thus, since the data is written into the register digit by digit at a period of (n−1) digits, the data is stored so as to be read out from the most significant digit down. The NAND gate NA4 is opened by the output of the changeover control circuit when the scale-of-n counter has counted n clock pulses, and the NAND gate NA1 is closed. If the NAND gate NA4 is opened, the clock signals ϕ_1 and ϕ_2 of the memory circuit 58 are synchronized with a clock pulse signal 30 for television picture display. Fig. 3 shows how the content of the operational register 4 of the ETC 78 is displayed on the picture tube of a television receiver. In this figure, (a) designates the content of the operational register 4 of the ETC 78, (b) the content of the register SR1 of the memory circuit 58, and (c) information displayed on the picture tube, where characters $A_1 \ldots A_n$ represent respective numerals beginning from the least significant digit and ending at the most significant digit. For example, as shown in the lower part of Fig. 3, when a number 123 is set in the ETC 78 the content of the operational register 4 of the ETC 78 is "00 . . . 123" as shown in (a)′, the content of the register SR1 of the memory circuit 58 is accordingly "321 . . . 00" as shown in (b)′, and the image displayed on the picture tube is therefore "123" as shown in (c)′.

Fig. 4 shows an example of the display control circuit 8 in Fig. 1 in detail. In this figure, an 8-bit counter 65 counts the horizontal sync signal 46 and can determine the horizontal position of the display on the picture tube by processing its respective outputs with appropriate logic circuits. Signals 26, 27, 28, and 29 determine the intervals of display in this four-way representation, a signal 80 determines the position of the line displayed on the picture tube, and a signal 81 serves as a clock signal to a row selecting circuit 66 which determines the rows in which certain characters are arranged on the picture tube. A decimal point determining circuit 67 determines the position of the decimal point in the ETC 78 by the signal 24 and supplies a decimal point signal 41 for the shift register 7. A gated oscillator 68 is an oscillator which is gated only during the duration of the horizontal sync signal and the clock pulse from this oscillator determines the horizontal position of the display. A spacing circuit 69 provides a space after every three digits to the left of the decimal point of the displayed numbers. The detail of the spacing circuit 69 will be described later. An 8-bit counter 70 counts clock pulses 75 obtained by dividing one horizontal sweep period (1H) by eight bits of a digit. A load signal 40 is delivered every time eight bits of the clock pulses 75 are counted and serves to write the data serially into the shift register 7 digit by digit. A flip-flop 72 determines the range of display of the line. Na10 to NA20 designate NAND circuit, AN1 to AN4 AND circuits, and IN1 to IN10 inverters.

The apparatus includes means for counting pulses of the horizontal sync signal contained in the second synchronizing signal and a means for generating a line signal when the number of counted pulses reaches a predetermined number so that a line is displayed between the operands and the computed result on the picture tube.

Fig. 5 shows the timings of the various signals appearing in the line display circuit, in which (a) represents the vertical sync signal 47 of the television system, (b) the horizontal sync signal 46, (c) the output of the AND circuit AN4, (d) the output of the NAND circuit NA19, (e) the output of the NAND circuit NA20, (f) the output 71 of the flip-flop 72, and (g) the output 42 of the NAND circuit NA18.

Fig. 6 shows the detailed constitution of the spacing circuit 69, in which are shown a scale-of-three counter 76, a delay circuit 77, a NAND circuit NA21, an AND circuit NA15, an inverter IN15, a clock signal 73 supplied for the 8-bit counter 70, a clear signal 74, a load signal 40 representing each digit, and a signal 75 obtained by gating the clock signal 73 at every three digits. The operation of the spacing circuit 69 is as follows. The scale-of-three counter 76 delivers an output signal to the delay circuit 77 every time it counts three pulses of the signal 40, the NAND circuit NA21 generates a pulse whose duration is equal to the delay time characteristic of the delay circuit 77, and the AND circuit AN15 gates the clock signal during the delay time. The timing relation between those signals mentioned above are shown in Fig. 7, in which (a) represents the load signal 40, (b) the output of the scale-of-three counter 76, (c) the output of the inverter IN15, (d) the output of the NAND circuit NA21, and (e) a clock signal 75 gated in response to the output (d).

Fig. 8 shows the timing chart of the input signals to the character generating circuit 6 and the parallel-series converting register 7,

Computer & TV displays simultaneously (1971)

in which (a) designates one of the outputs 36, 37, 38 and 39 carrying numeral information of the data converting circuit 5, (b) the output waveform giving the pattern of a numeral delivered from the charcater generating circuit 6 in response to the output signal 36, 37, 38 or 39, (c) the load signal 40, (d) the clock signal 30, and (e) a numeral pattern (5×7). For example, in this case, if a row is determined as "OC1" and the input data to the character generating circuit 6 is "1", the outputs 51, 52, 53, 54 and 55 will be 0, 0, 0, 1, 0, respectively. The position of clock signals 30 relating to signals representing the numeral pattern are indicated by the dash lines between (d) and (e).

Fig. 9 shows the circuit of an example of the color control circuit 9 in Fig. 1, in which NA22 to NA25 are NAND circuits and IN11 to IN14 are inverters. A signal 43 as a dot signal representing a numeral pattern is fed to both the NAND circuits NA22 and NA24, and if the input data 43 is identical with the memory value that is, the contents of the memoriy in the computipseretion, i.e., ETC., the NAND circuit NA22 is opened by the signal 29. If the output 45 of the NAND circuit NA22 is applied to, for example, the red output circuit of the matrix circuit 17, the memory value displayed in the uppermost row on the picture tube luminesces in red. If, on the other hand, the signal 43 is different from the memory value, the signal 43 is passed through the NAND circuit NA24 and fed to the NAND circuit NA25, which takes the logic sum of the signal 43 and the line signal 42. If the output 44 is applied to, for example, the green output circuit of the matrix circuit 17, the numerals indicating the process of computation luminesce in green.

In Fig. 10, diagram (a) shows the positions of the information displayed on the picture tube, in which the memory value is located in the uppermost or first row, the operand in the second row, the operator and operand in the third row, and the computed result in the fourth row.

The diagram (b) shows an Example of actual computation on the picture tube of a television receiver.

Fig. 11 shows as an example the steps of the whole process of an actual computation on the picture tube of a television receiver, in which (i) designates the step of displaying the operand "12", (ii) the step of adding the operator "X", (iii) the step of adding the operand "4", (iv) the step of pushing the equal button, (v) the step of storing the computed result "48" in the memory circuit that is to say in the fourth of the registers SR1, SR2, SR3 and SR4, and (vi), (vii), (viii) and (ix) the steps of performing the computation "24−48=". When the number as the computed result or the memory value takes a negative value, it is preceded by an algebraical sign "−".

As described above there are obtained various advantages such as the possibility of checking a computing process during the comptation, the moment-to-moment display of the content of the memory register, the clarification of the computing process and the computed result by the use of multi-color representation, the display of a line or lines in the computing proces, the provision of spaces between every third and fourth digits, and the display of the computed information on the picture tube of a television receiver in superposition with the television program.

It will be seen that apparatus embodying the present invention enables the display of a computing process by employing what is called multiple-row-display.

Again embodiments of the present invention provide a simple data converting means for displaying a computing process on a picture tube without unifying the timing system of the ETC with that of the display system.

Further, embodiments of the present invention provide a means for inserting a line between the numerals to be processed and the computed result in the display in order to make the computing process more comprehensible.

Again, embodiments of the present invention provide a means for making in each displayed number a space on the left of every third digit appearing to the left of the decimal point in order to facilitate reading the result in the same manner as in a number with commas applied every three digits. embodiments of the present invention, further provide a color control means enabling display of the numbers from the memory in different colors from the other numbers in the calculation so as to make the display distinct.

The present invention also provides a television receiver on the picture tube of which a television program and the result of the computing process are shown simultaneously.

Yet another advantage of embodiments of the present invention is the provision of apparatus in which a memory value is displayed in the uppermost row, an operand (such as an addend, minuend, multiplicand or dividend) is displayed in the second row, an operator or calculating sign and an operand (such as an augend, subtrahend, multiplier or divisor) are displayed in the third row, and the computed result is displayed in the fourth row.

WHAT WE CLAIM IS:—

1. An apparatus for displaying a computing process comprising a computing means for performing a computing operation on

input data, a memory means for storing the input data and result of the computing process performed by said computing means, a means for reading the contents of said memory means and converting said contents into charcater representative video signals, a means for receiving a television signal and demodulating the video signal in the received television signal, a picture tube operated to display thereon images by receiving said character representative video signals and the signal from said receiving and demodulating means, wherein the images represented by the character representative video signals and the demodulated video signal are displayed in superimposition on the picture tube, a driving means which receives a first synchronizing signal obtained from said computing means and a second synchronizing signal separated from said television signal and which applies to the memory means driving pulses timed in relation to the timing either of said first synchronizing signal in the case of writing into said memory means or of said second synchronizing signal in the case of reading of the contents of said memory means.

2. Apparatus according to claim 1, wherein said memory means includes a register having a storage capacity of $4 \times n$ bits, where n is the number of digits of the result of the computing process and each digit is represented by 4 bits, said driving means includes a counter for delivering a clock pulse every time it counts $4 \times (n-1)$ pulses of said first synchronizing signal and a means for generating said driving pulses in response to said clock pulses, and wherein the result of the computing process is obtained from said computing means, starting from the least significant digit, and the digits are written into said register in such positions that they may be read out starting from the most significant digit.

3. Apparatus according to Claim 1, wherein there is provided a means for counting pulses of a horizontal sync signal separated from the television signal and wherein the digits represented by said character representative video signals are arranged on said picture tube with an appropriate space left therebetween by reading out of said memory means parts of the stored information when the number of counted pulses reaches a predetermined number.

4. Apparatus according to Claim 2 wherein said memory means includes two further registers each having a storage capacity of $4 \times n$ bits, information from the computing means is selectively applied respectively to said three registers to store therein the operands and the computed result, and wherein the operands and the computed result are displayed on said picture tube by reading the contents of said registers.

5. Apparatus according to Claim 4, wherein there is provided a means for counting pulses of a horizontal sync signal contained in said second synchronizing signal and a means for generating a line signal when the number of counted pulses reaches a predetermined number, so that a line is displayed between said operands and said computed result on said picture tube.

6. Apparatus according to Claim 1, wherein there is provided a means for counting the digits of the contents read from said memory means from the least significant digit upwards in groups of three digits and a means for gating said driving pulses applied to said memory means for the purpose of reading in response to the output of said counting means, so that spaces are provided between every third and fourth least significant digit of each number displayed on said picture tube.

7. Apparatus according to Claim 4, wherein said picture tube is a colour picture tube and a means is further provided for displaying the operands and the computed result in different colors and in a plurality of rows on said color picture tube.

8. Apparatus according to Claim 4, wherein said memory means consists of four registers for storing therein a memory value, a first operand, a second operand, and the computed result, and wherein the stored information is then read out to be displayed in four rows in the order mentioned on said picture tube.

9. Apparatus substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

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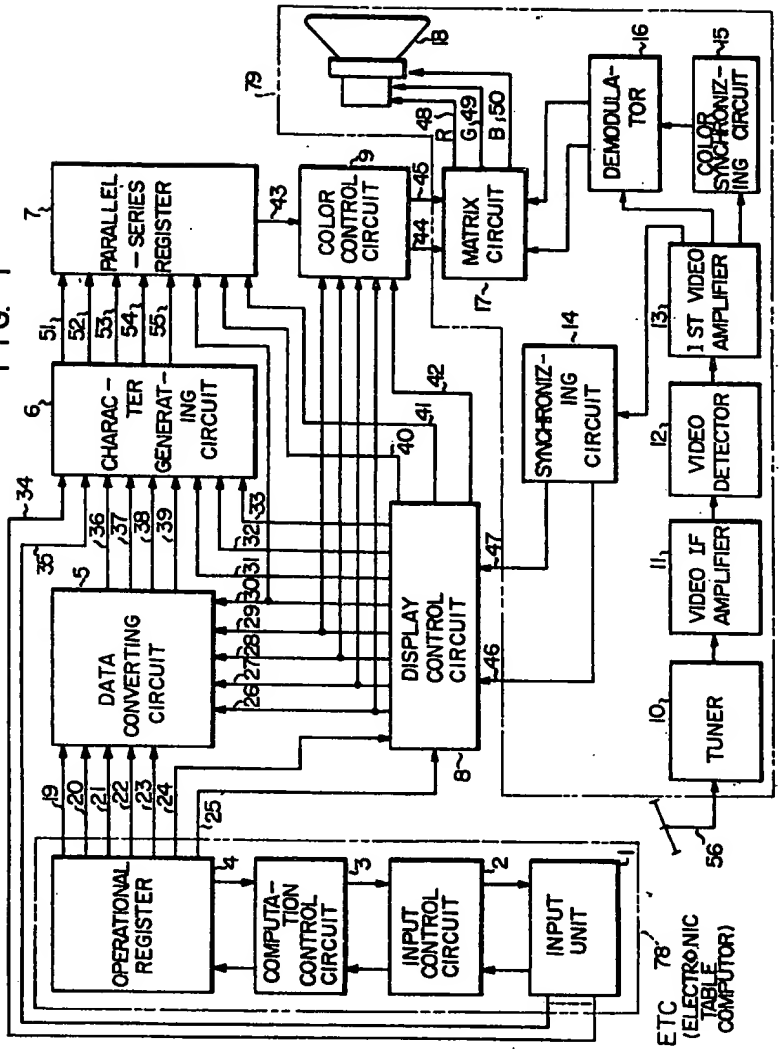
1405141 COMPLETE SPECIFICATION
10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

FIG. 1



1405141 COMPLETE SPECIFICATION
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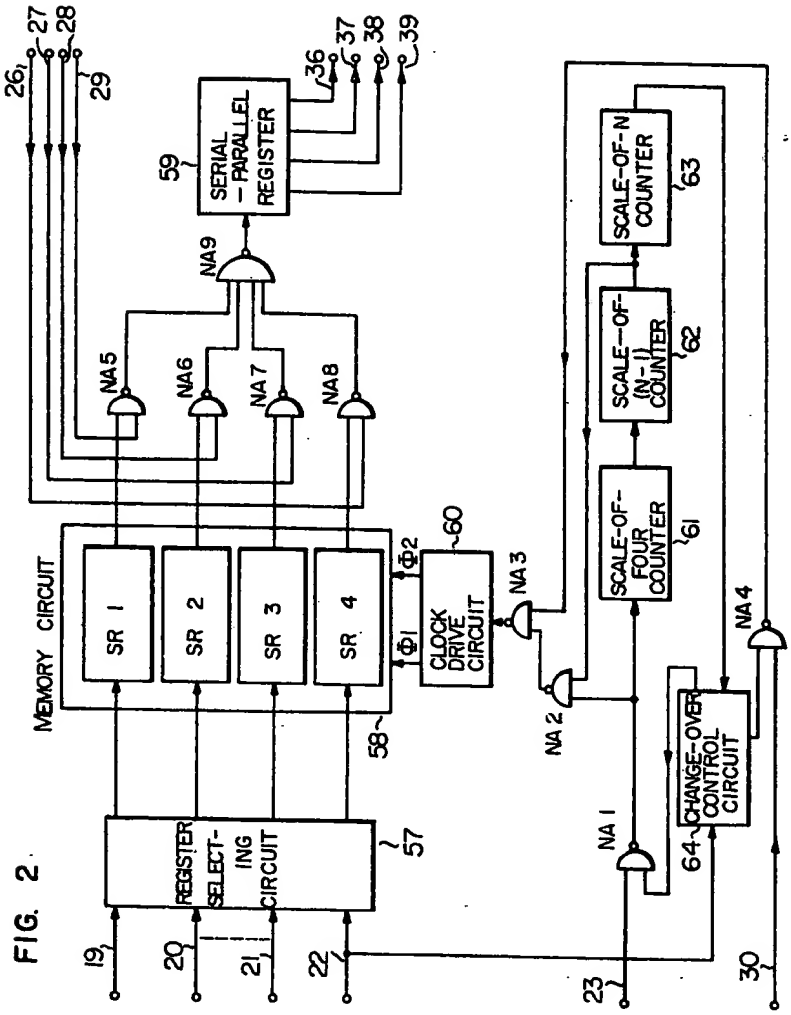
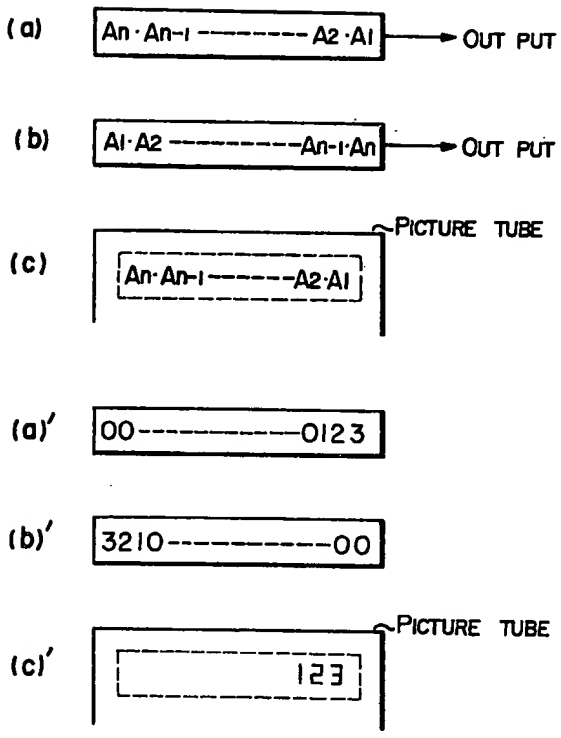


FIG. 2

FIG. 3


(a)
An·An-1 --------A2·A1
OUT PUT
(b)
A1·A2 ---------An-1·An
OUT PUT
(c)
PICTURE TUBE
An·An-1------A2·A1
(a)'
00----------0123
(b)'
3210----------00
(c)'
PICTURE TUBE
123

1405141 COMPLETE SPECIFICATION
10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 4

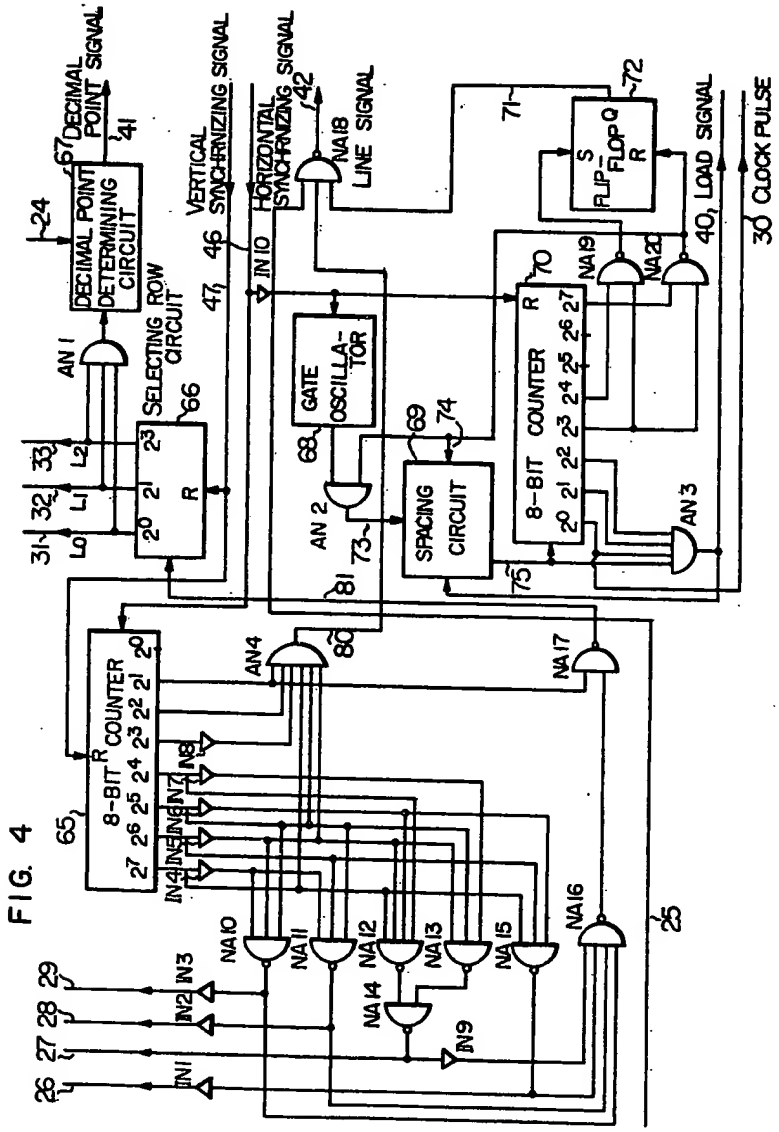


FIG. 4

FIG. 5

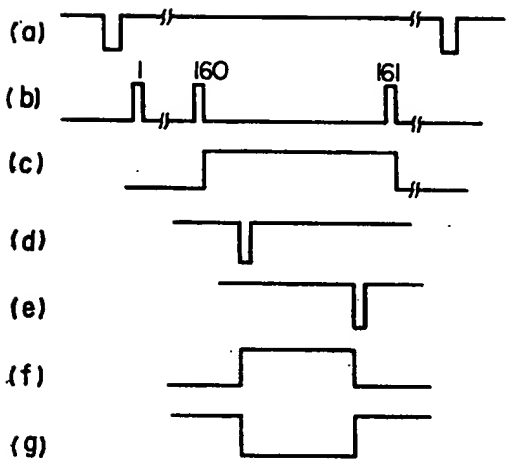
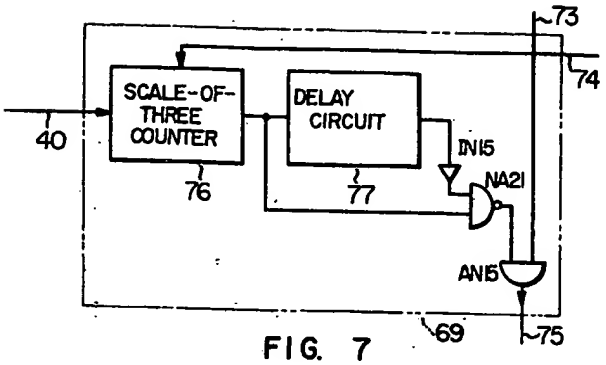


FIG. 6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74
SCALE-OF-THREE COUNTER
DELAY CIRCUIT
40
IN15
NA21
AN15
76
77
69
75

FIG. 7

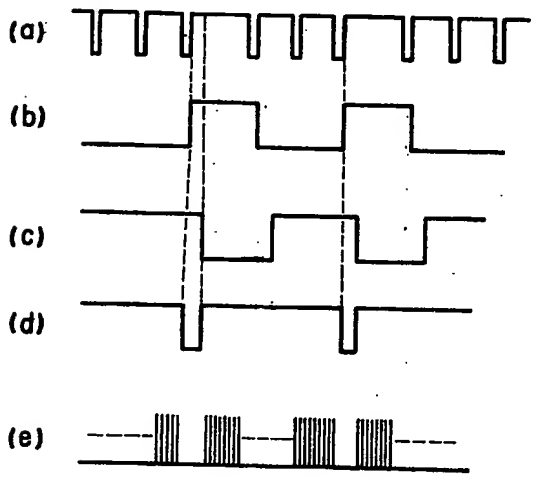

(a)
(b)
(c)
(d)
(e)

FIG. 8

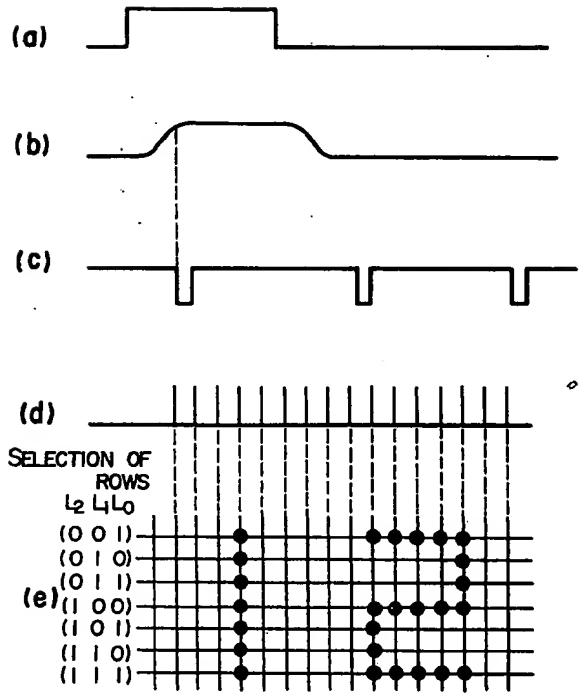


FIG. 9

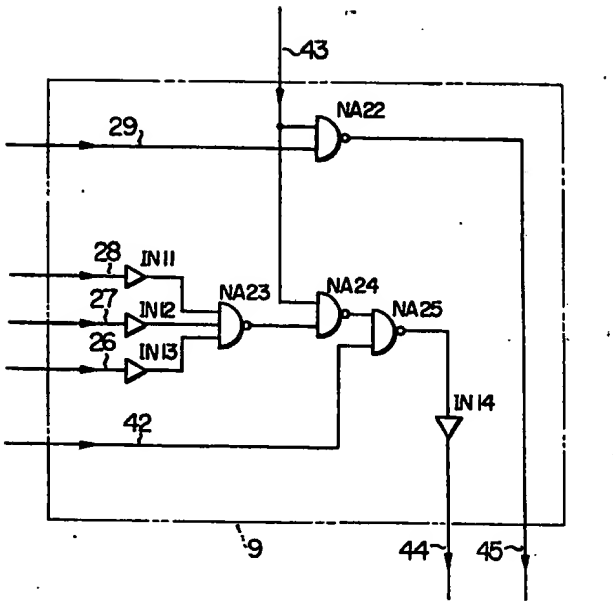
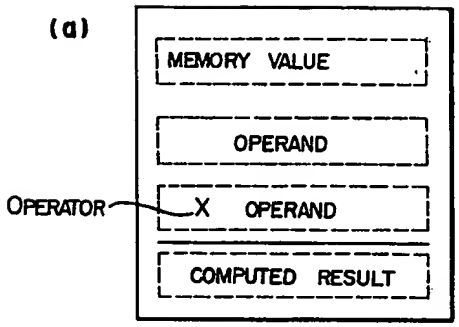


FIG. 10



(EXAMPLE) MEMORY VALUE: 12.345

COMPUTATION: 23758.4+3.2=23761.6

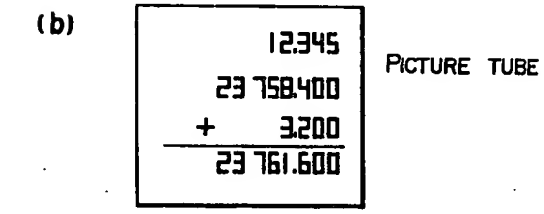
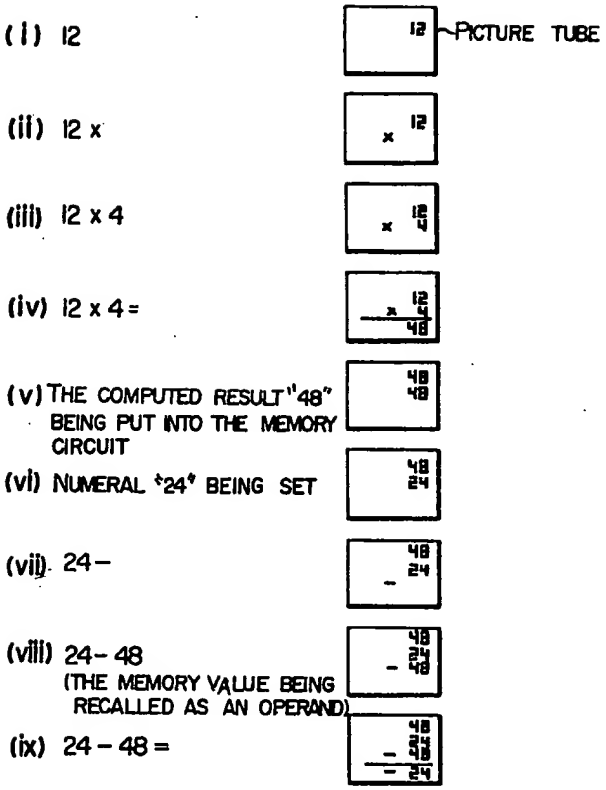


FIG. 11


(i) 12
12
PICTURE TUBE
(ii) 12 x
x 12
(iii) 12 x 4
x 12 4
(iv) 12 x 4 =
x 12 4 48
(v) THE COMPUTED RESULT "48" BEING PUT INTO THE MEMORY CIRCUIT
48 48
(vi) NUMERAL "24" BEING SET
48 24
(vii) 24 –
48 – 24
(viii) 24 – 48
(THE MEMORY VALUE BEING RECALLED AS AN OPERAND)
48 – 24 48
(ix) 24 – 48 =
48 – 24 48 – 24